# DIGITAL SIGNAL PROCESSING MODULE DSP-3U-SH201

(brief technical description)

Year of manufacture: 2012
Part number: DSP-3U-SH201
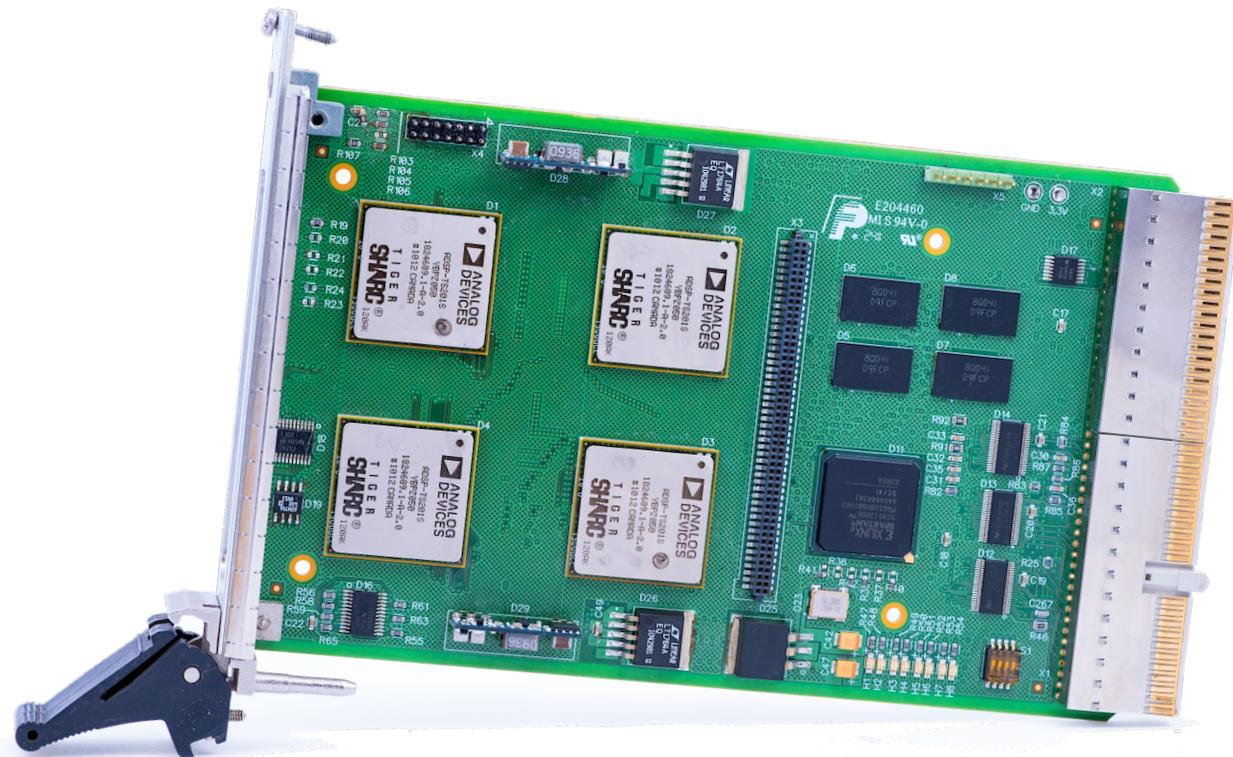
powered by Analog Devices SHARC®

FLASH 64Mb

SRAM 128MB

64 bits

64 bits

L0 L2 / L2 L0
L3 P2 P3 L3
L1 L1

L0

EXTERNAL MEZZANINE

L1
L2

L1 L2 / L1 L1
L3 P1 P4 L3
L0 L0

L3

FPGA
BRIDGE

L0 L1 L2 L3 PCI

CompactPCI
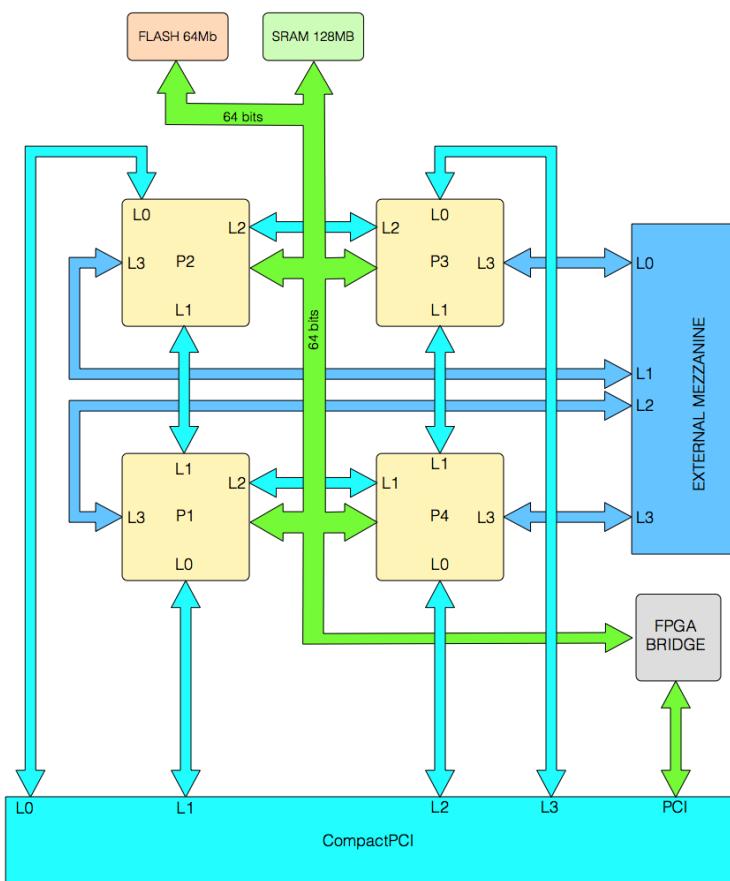
Function

The DSP-3U-SH201 is a multiprocessing device that designed with using of four signal processors DSP-3U-SH201 of TigerSHARC® family and is intended for a real-time digital signal processing building.

Key features

Four processors that have summarized computational power 9,6 GFLOPS, are being switched in the parallel 64-bits electrical data bus (100MHz clock) and four 4-bits high-speed pipe-lines of LINK-ports (400MHz clock). The parallel data bus supplies a data access for each DSP to the SRAM memory space (128Mb) and to the Flash memory space (64Mb). Each DSP has a direct LINK port connection with cPCI user interface (1-bit) and PMC mezzanine interface (4-bits).

Design

The module is shaped according to 3U CompactPCI standard. The module has two basic interfaces for data input/output organization. To ensure additional protection against environmental influences, all module surfaces are covered with a conformal waterproof coating.

Input/output CompactPCI and Mezzanine data interface

The user cPCI connector and mezzanine connector have:
 four LINK port interfaces that operate with LVDS standard (1-bit bus width for cPCI interface and 4-bits for mezzanine one); flag i/o and interrupt input pins; the Watchdog system i/o pins; clock signal pins (100MHz).

Developer tools

For the program debugging of user software the module has JTAG interface fully matched to Analog Devices emulators of ICE family and development tools such as Analog Devices VisualDSP++® or Analog Devices CrossCore®.

In order to user loading software building, board failure checking and flash reprogramming there is a ToolKitDSP® utility.

MAIN SETTINGS	
Parameter Name	**Value**
Computational power	9.6 GFLOPS
Numbers of DSP	4
Processors type	SHARC ADSP-TS201
Bus clock	100MHz
DSP clock	400MHz
DSP internal memory	4 x 24Mb
SRAM memory	128MB
FLASH memory	64Mb
Number of led indicators	8(green)
Number of Interrupt inputs	2
Number of flag inputs/outputs	8
Data transfer rate, max:	
Mezzanine LINK buses	4 x 200MB/s = 800MB/s
CompactPCI LINK buses	4 x 50MB/s = 200MB/s
Supply voltage:	
Nominal	3,3 V
Min	3,13 V
Max	3,47 V
Power consumption	
Nominal	20 W
Max	30 W
Dimension	160 x 100 mm
Outline dimension	4HP 3U PIGM 2.0.
Developer tools	AD VisualDSP++® , AD CrossCore® HPUSB-ICE, HPPCI-ICE, ICE-1000, ICE-2000 ToolKitDSP
Temperature range	- 40℃ …+70℃
Additional environmental protection	Conformal waterproof coating