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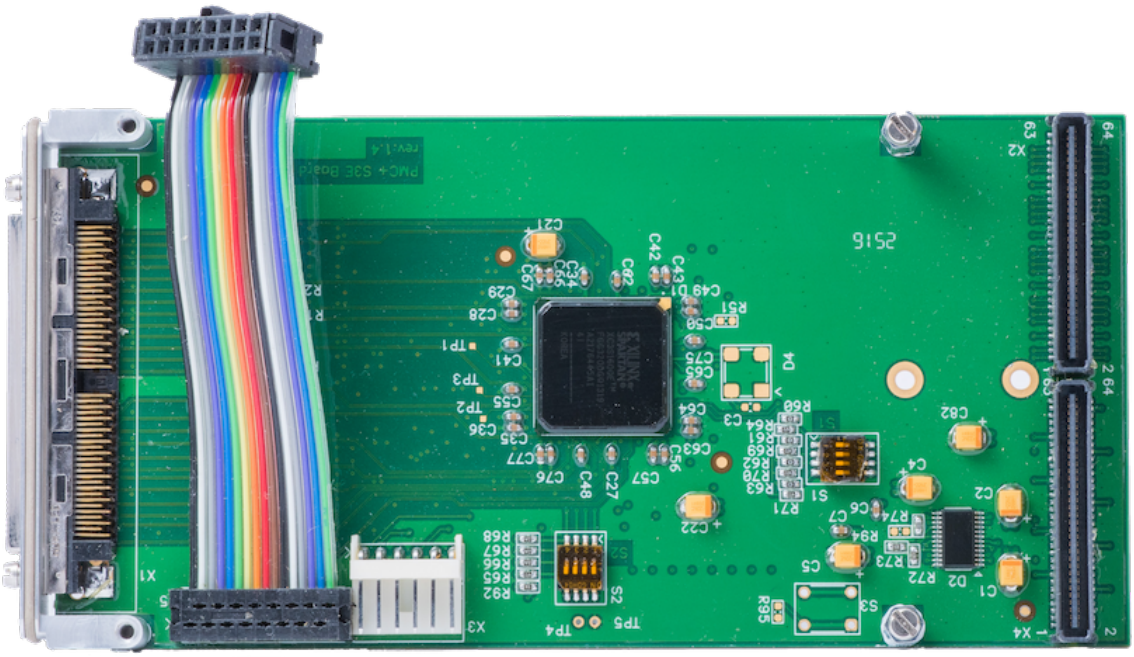
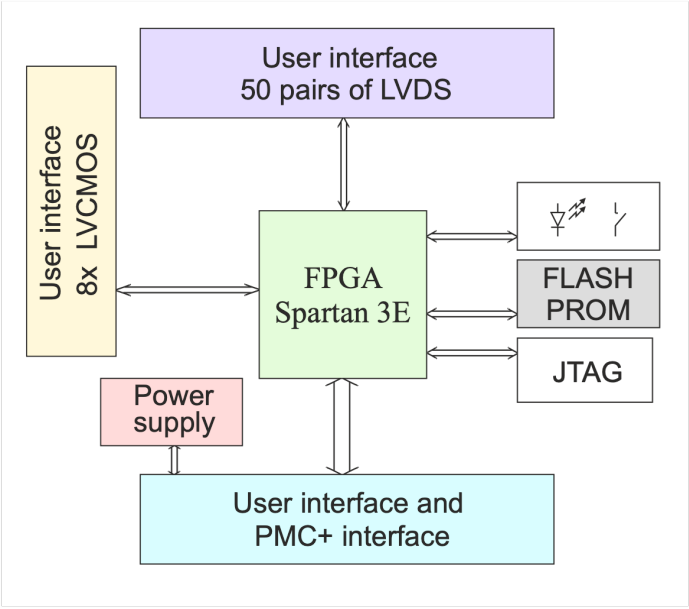
DIGITAL SIGNAL PROCESSING MODULE S3EX-PMC-02

(brief technical description)

Year of manufacture: 2010

Part number: S3EX-PMC-02





Function

The S3EX-PMC-02 is a programable logical computing device intended for digital signal processing.

The module was designed with a FPGA Spartan® 3E, that is used for real-time signal processing application.

Key features

Computational resource FPGA Xilinx Spartan® 3E is based on 1,6 logical units.

The module has a FLASH memory (32Mb), that is used for automatic configuration FPGA resource by user program.

Design

The module is shaped according to Draft Standard for a Common Mezzanine Card Family: CMC (P1386/Draft 2.4a) and the extension of a single format CMC. The basic external input-output interfaces are: a main hight-density connector placed at the front of the board, expansion connectors of PMC+ interface and user connector fixed with a flexible flat cable.

To ensure additional protection against environmental influences, all module surfaces are covered with a conformal waterproof coating.

I/O data interface

The data interface is represented with hight-density connector placed at the front of the board and can transfers up to 50 LVDS signals.

Developer tools

There is a debugging interface connector (JTAG) on the board, intended for user program running. That interface is fully matched to be used with configuration cables like Platform Cable USB (p/n: HW-USB-G, p/n: HW-USB-II-G) by Xilinx and Xilinx iMPACT utility. The basic software that is used for the module software developing including the flash images is Xilinx Foundation®.

MAIN SETTINGS	
Parameter Name	**Value**
Number of LVDS pairs (in the I/O data connector)	50
Number of configurable I/O lines (in the rear connector) LVDS/LVCMOS	44
Electrical signal standard of data bus	LVDS25, LVCMOS25
Number of logical units	76x58 (3 688)
Maximum volume of distributed RAM, KB	231
Maximum volume of Block RAM (550MHz), MB	648
Number of multiplier units (18x18)	36
Number of equal logic units	33 192
Number of FPGA Spartan 3E chips	1
Number of PMC+ connectors	2
Flash memory size, Mb	8
Power consumption, not more, W	3
Size	149 x 74 mm
Outline dimension	According to Draft Standard for a Common Mezzanine Card Family: CMC (P1386/Draft 2.4a).
Developer tools	Xilinx iMPACT® , Xilinx ISE Foundation®
Temperature range	-40˚C …+65˚C
Additional environmental protection	Conformal waterproof coating