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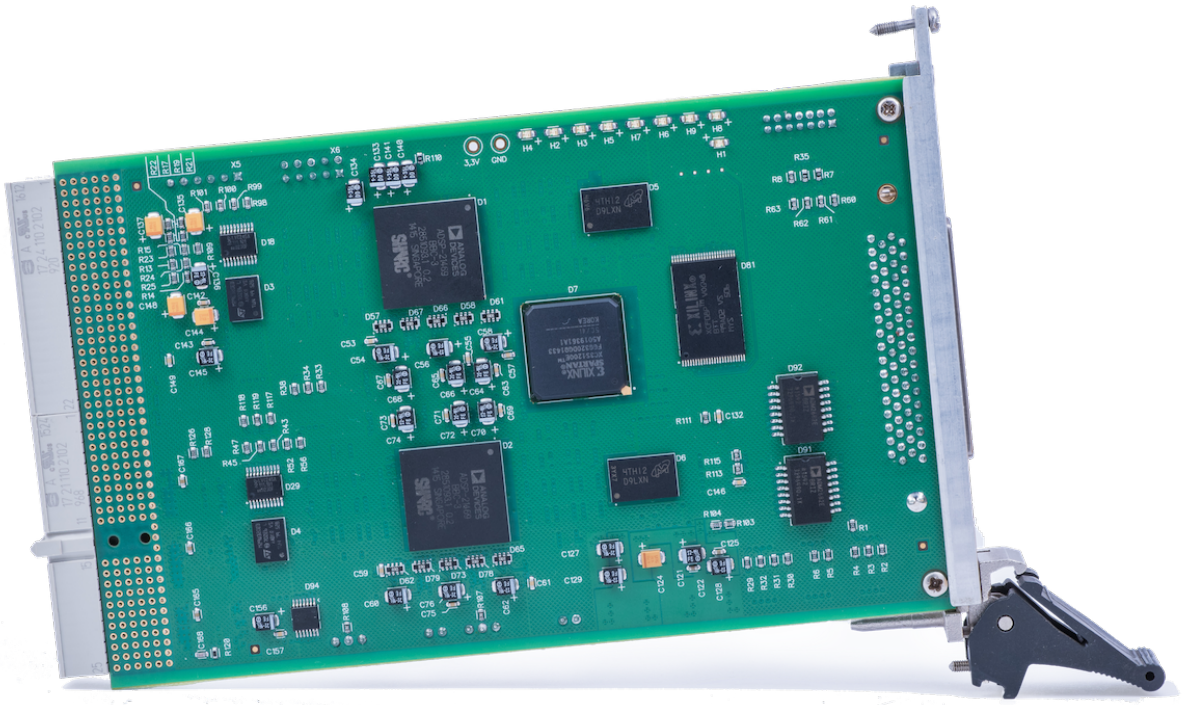
DIGITAL SIGNAL PROCESSING MODULE DSP-3U-SH469

(brief technical description)

Year of manufacture: 2018
Part number: DSP-3U-SH469



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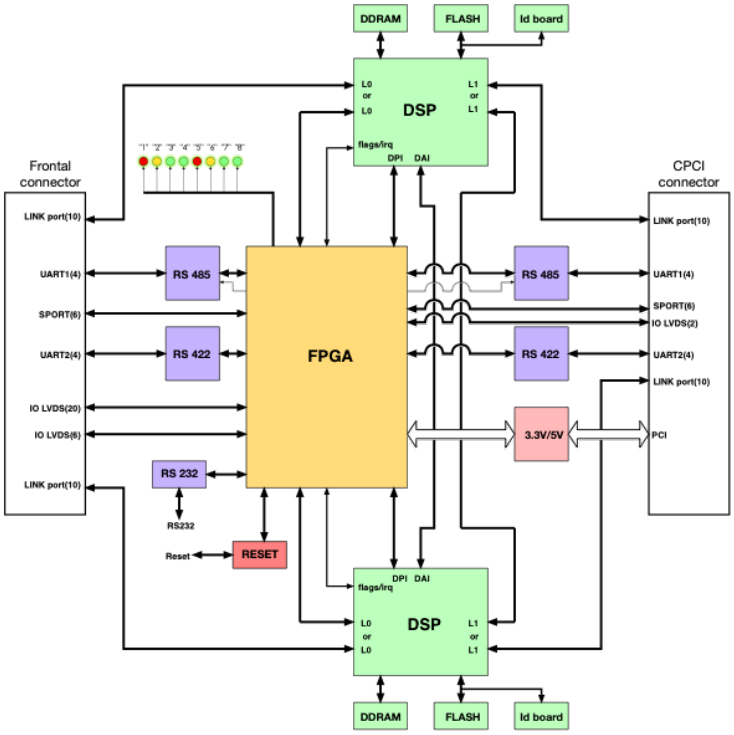

Function

The DSP-3U-SH469 is a multiprocessing device designed with using of two signal processors ADSP-21469 of SHARC® family and FPGA Xilinx Spartan®-3E family that is intended for a real-time digital signal processing building.

Key features

Two processors have summarized computational power 5,4 GFLOP create series-parallel chain of data processing optimized for up-to-date radar applications.

Each DSP has his own 128MB RAM memory and 32Mb FLASH memory with monopoly access. The data exchange between processors occurs through the LINK-port interface and six SPORT interfaces.

The FPGA installed between DSPs is realized bridge functions and helps to manage different kind of external I/O data interfaces like isolated RS-422/485 and LVDS on different pins of external connectors.

The most important feature of the module is a presence of wide software support that supplies a real-time access to DSP resources and programming interface.

Design

The module is shaped according to 3U CompactPCI standard. The module has two external connectors: a frontal har-mik® connector and CompactPCI back connector.

To ensure additional protection against environmental influences, all module surfaces are covered with a conformal waterproof coating.

Input/output CompactPCI data interface

User part of CPCI connector contains two Link-ports, Serial port in TDM mode, isolated RS-422/485 interface, flag and interrupt processor pins, WATCHDOG input/output pins, system clock output pin (25 MHz).

Input/output frontal interface

Frontal connector has two Link-ports, single Serial port (SPORT) and thirteen configurable LVDS lines, that can be programmed according to the target-system architecture.

Developer tools

For the program debugging of user software the module has JTAG interface fully matched to Analog Devices emulators and development tools such as Analog Devices VisualDSP++® or CrossCore®.

Additionally there is a set of user and developer software supplied with the module - libDSP®. Programs and developer libraries allow to develop programs with board resource managing, load user programs to the FLASH memories, to have an access to DSP memory in real-time mode.

CRITICAL PARAMETERS	
Parameter Name	**Value**
Computational power	5,4 GFLOPS
Numbers of DSP	2
Type of processor	SHARC ADSP-21469
DSP clock	450MHz
DSP internal memory	2 x 5Mb
DDR memory	2 x 128MB
FLASH memory	2 x 32Mb
Number of led indicators	2 x 4
Number of Interrupt inputs	adjustable, up to 5
Number of flag inputs/outputs	adjustable, up to 13
Data transfer rate, max:	
LINK buses	4 x 166MB/s = 664MB/s
SPORT lines	10 x 50Mb/s
UART buses	2 x 921kb/s (RS-422/485) 1 x 230kb/s (RS-232)
Supply voltage:	
Nominal	3,3 V
Min	3,13 V
Max	3,47 V
Power consumption:	
Nominal	3 W
Max	7 W
Dimension	160 x 100 mm
Outline dimension	4HP 3U PIGM 2.0.
Developer tools	AD VisualDSP++® , AD CrossCore® HPUSB-ICE, HPPCI-ICE, ICE-1000, ICE-2000 libDSP®
Temperature range	-40˚C …+70˚C
Additional environmental protection	Conformal waterproof coating

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